Unit 9: Multiplexers, Decoders and Programmable Logic Devices

9.1 Introduction

Complex integrated circuits for design

- Small Scale Integration - SSI
  - Use NAND, NOR, AND, OR, Invertors and Flip Flops
  - 1 – 4 Gates, 6 Invertors and 1 – 2 Flip Flops

- Medium Scale Integration - MSI
  - Adders, Multiplexers, Decoders, Counters
  - 12 – 100 Gates

- Large Scale Integration - LSI
  - More complex 100 – few thousand gates

- Very Large Scale Integration – VLSI
  - Several thousand gates

9.2 Multiplexers

Multiplexer (MUX) – has a group of data inputs and a group of control inputs where the control inputs select which of the data inputs connect to the ouput terminal.

MUX act like a switch that selects a data input and transmits the output.

4-to-1 MUX: 4 data inputs and 2 control inputs

$$Z = A'B'I_0 + A'BI_1 + AB'I_2 + ABI_3$$

8-to-1 MUX: 8 data inputs and 3 control inputs

$$Z = A'B'C'I_0 + A'B'CI_1 + A'BC'I_2 + A'BCI_3 + AB'C'I_4 + AB'CI_5 + ABC'I_6 + ABCI_7$$

2^n-to-1 MUX: 2^n data inputs and n control inputs

Where m_k is the minterm of the n control variable and I_k is the corresponding data input

Quadruple 2 – to – 1 MUX

Quad MUX

9.3 Three-State Buffers

Buffer: device used to increase the driving capacity of a gate output.

Three-state buffer (tri-state buffer): permits the outputs of two or more gates or logic devices to be connected together.

4 Kinds of Three-State Buffers

Data Selection using Three-State Buffers

Circuit with Two Three-State Buffers

Integrated Circuit with Bi-Directional Input/Output Pin

9.4 Decoders and Encoders

3-to-8 Line Decoder

4-to-10 Line Decoder

In general, an n-to-2^n line decoder generates all the minterms (Maxterms) of the n input variable.
Where the outputs $y_i = m_i$ for I = 0 to 2^n -1

An encoder performs the inverse function of a decoder.

9.5 Read-Only Memories

Read-only memory (ROM) – An array of semiconductor devices that interconnect to store an array of binary data.

- Stored data can be read anytime but can not be readily changed
- For each combination of input values a corresponding value of ones and zeros appear as an output

Word – Each output pattern that is stored

Address – Each input combination, used to select output word

A	B	C	F_0	F_1	F_2	F_3
0	0	0	1	0	1	0
0	0	1	1	0	1	0
0	1	0	0	1	1	1
0	1	1	0	1	0	1
1	0	0	1	1	0	0
1	0	1	0	0	0	1
1	1	0	1	1	1	1
1	1	1	0	1	0	1

A ROM with n inputs and m outputs has 2^n words each m bits long

A 2^n X m ROM can realize m functions of n variables in a truth table of 2^n rows and m columns

Basic ROM structure – A decoder and a memory array.

When 1's and 0's are applied to the n inputs exactly one of the 2^n decoder outputs is 1.

The decoder output selects a word from the memory array and transmits it to the output.

Switching elements are placed at the intersection of word lines and output lines if a minterm is part of the output. If a switching element connects a word line to an output line which is 1, the output line will be 1 else the pull down resistor causes the output to be 0.

$$F_0 = \sum m\,(0,1,4,6) = A'B' + AC'$$

$$F_1 = \sum m\,(2,3,4,6,7) = B + AC'$$

$$F_2 = \sum m\,(0,1,2,6) = A'B' + BC'$$

$$F_3 = \sum m\,(2,3,5,6,7) = AC + B$$

A hexadecimal to ASCII converter

Because A4 = A5 and A6 = A4' the ROM needs only 5 outputs because there are 4 address lines the ROM size is 16 words by 5 bits

ROM realization of code converter

An X indicates a switching element at the intersection of a row and a column.

Types of ROM

1. Mask-programmable ROM
    a. Data is stored at the time of manufacturing

    b. Requires preparation of special mask during fabrication

    c. Expensive, only economical in large quantities

2. Programmable ROM (PROM)

3. Electrically Erasable Programmable ROM (EEPROM)

    a. Useful since data may need to be modified during developmental phases of design

    b. Special charge storage mechanism is used to enable or disable switching elements in memory (PROM programmer)

    c. Data is permanent until erased (limited number of times to be erased and reprogrammed, 100-1000)

4. Flash memory- similar to EPROM except have a built in erase and program capability, doesn't require a separate programmer

9.6 Programmable Logic Devices

Programmable Logic Devices (PLD) – General name for digital integrated circuit capable of being programmed for a variety of different logic functions

Programmable Logic Array (PLA) –Performs same function as a ROM. Internally the decoder is replaced with an AND array and an OR array. OR's the product terms to form the output function.

The PLA implements an SOP expression; ROM directly implements a truth table

To form A'B' switching elements connect the first word line with A' and B'. Switching elements are connected in the OR array to select the product terms needed for the output function.

$F_1 = a'bd + adb + ab'c' + b'c$ $F_2 = c + a'bd$ $F_3 = bc + ab'c' + abd$

Masked-programmable PLA: programmed at the time of manufacture

Field-programmable PLA: uses electronic charge to store a pattern on the AND and OR arrays

PROM's are economical for a small number of inputs otherwise PLA's are most the economical solution

Programmable Array Logic (PAL): special case of a PLA where the AND array is programmable and the OR array is fixed.

Note: Structure similar to the PLA but less expensive and easier to program.

When a PAL is programmed, connections to the AND gates are shown by X's

Design Notes: Try to fit the logic equation to the available PAL. Gates cannot be shared, simplify without worrying about common terms.

Implementing a Full Adder

$$Sum = X'Y'C_{in} + X'YC_{in}' + XY'C_{in}' + XYC_{in}$$

$$C_{out} = XC_{in} + YC_{in} + XY$$

9.7 Complex Programmable Logic Devices

Complex programmable Logic Device (CPLD): single IC chip which contains multiple interconnected PLA's and PAL's that implement a small digital system

9.8 Field Programmable Gate Arrays

Field Programmable Gate Arrays (FPGA): IC that contains an array of identical logic cells with programmable interconnections. The user can program the functions of each logic cell and the connection between cells.

Decomposition of Switching Functions

Shannon's expansion theorem

Karnaugh Map

cd \ ab	00	01	11	10
00	1	1	1	1
01			1	1
11	1	1	1	
10	1			

cd \ ab	00	01	11	10
00	1	1	1	1
01			1	1
11	1	1	1	
10	1			

5-variable function

6-variable function (use the theorem twice)

Alternate: